## Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the subject application.

## Listing of Claims:

1. (Currently Amended) A system comprising:

a core processing circuit; and

a host processing system coupled to the core processing circuit through a host bridge, the host processing system comprising:

logic to maintain the core processing circuit in a reset state during power up of the core processing circuit; and

logic to load a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions to initialize the core processing circuit upon release from the reset state;

wherein the host processing system further comprises a system memory and logic to set an address translation unit to enable at least one outbound transaction to address at least one location in the system memory to fetch instructions from the system memory in response to requests from the core processing circuit, the address translation unit being configured to convert an internal data bus address associated with the outbound transaction to an external data bus address and configured to forward the outbound transaction from an internal data bus coupled to the core processing circuit to an external data bus coupled to the system memory.

2. (Original) The system of claim 1, wherein the registers are formed in one of a cache memory array associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus.

3. (Original) The system of claim 1, wherein the host processing system comprises a system memory, and wherein the reset vector comprises at least one instruction to fetch data from a system memory coupled to the core processing circuit through the host bridge.

4. (Cancelled)

5. (Previously Presented) The system of claim 3, wherein the host processing system further comprises logic to initiate one or more write bus transactions at an address translation unit to load the reset vector in the registers while the core processing circuit is in the reset state, and wherein the core processing circuit comprises logic to initiate one or more read bus transactions at the address translation unit addressed to the system memory in response to execution of the reset vector upon release from the reset state.

6. (Original) The system of claim 1, wherein the host processing system further comprises logic to release the core processing circuit from the reset state in response to loading the reset vector at the boot address.

7. (Original) The system of claim1, wherein the additional instructions comprise instructions to commence a power-on self test procedure.

8. (Previously Presented) The system of claim 7, wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit.

9. (Currently Amended) A method comprising:

having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit;

loading a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions from a system memory coupled to the core processing circuit through a host bridge of a host processing system; ~~and~~

setting an address translation unit to enable at least one outbound transaction to address at least one location in the system memory to fetch instructions from the system memory in response to requests from the core processing circuit~~.~~; and

in response to an outbound transaction, converting an internal bus address associated with the outbound transaction to an external data bus address and forwarding the outbound transaction from an internal data bus coupled to the core processing circuit to an external data bus coupled to the system memory.

10. (Original) The method of claim 9, the method further comprising loading the reset vector to a boot address in registers formed in one of a cache memory associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus.

11. (Cancelled)

12. (Previously Presented) The method of claim 9, wherein the method further comprises:

initiating one or more write bus transactions at an address translation unit to load the reset in the registers while the core processing circuit is in the reset state; and

initiating one or more read bus transactions at the address translation unit addressed to the system memory in response to execution of the reset vector upon release of the core processing circuit from the reset state.

13. (Original) The method of claim 9, wherein the additional instructions further comprise instructions to commence a power-on self test procedure.

14. (Original) The method of claim 13, wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit.

15. (Currently Amended) A method comprising:

having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit;

loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit, the instructions comprising one or more instructions to initialize the core processing circuit upon release of the core processing circuit from the reset state; ~~and~~

setting an address translation unit to enable at least one outbound transaction to address at least one location in the system memory to fetch instructions from the system memory in response to requests from the core processing circuit~~.~~; and

in response to an outbound transaction, converting an internal bus address associated with the outbound transaction to an external data bus address and forwarding the outbound transaction from an internal data bus coupled to the core processing circuit to an external data bus coupled to the system memory.

16. (Original) The method claim 15, wherein the method further comprises transmitting the instructions from the system memory through a host bridge of the host processing system.

17. (Original) The method of claim 15, the method further comprising releasing the core processing circuit from the reset state in response to loading the instructions at the boot address.

18. (Original) The method of claim 15, the method further comprising loading the instructions to a boot address in registers formed in one of a cache memory associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus.

19. (Cancelled)

20. (Previously Presented) The method of claim 15, wherein the one or more instructions comprise instructions to commence a power-on self test procedure.

21. (Previously Presented) The method of claim 20, wherein the one or more instructions further comprise instructions to launch an operating system to the core processing circuit.

22. (Currently Amended) An article comprising:

a storage medium comprising machine-readable instructions encoded there on for:

having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit;

loading a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions from a system memory coupled to the core processing circuit through a host bridge of a host processing system; and

setting an address translation unit to enable at least one outbound transaction to address at least one location in the system memory to fetch instructions from the system memory in response to requests from the core processing circuit, the address translation unit being configured to convert an internal data bus address associated with the outbound transaction to an external data bus address and configured to forward the outbound transaction from an internal data bus coupled to the core processing circuit to an external data bus coupled to the system memory.

23. (Original) The article of claim 22, wherein the storage medium further comprising machine readable instructions stored thereon for loading the reset vector to a boot address in registers formed in one of a cache memory associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus.

24. (Cancelled)

25. (Original) The article of claim 22, wherein the storage medium further comprises machine readable instructions stored thereon for initiating one or more write bus transactions at an address translation unit to load the reset vector in the registers while the core processing circuit is in the reset state.

26. (Original) The article of claim 22, wherein the storage medium further comprises machine readable instructions stored thereon for releasing the core processing circuit from the reset state in response to loading the reset vector at the boot address.

27. (Original) The article of claim 22, wherein the additional instructions comprise instructions to commence a power-on self test procedure.

28. (Original) The article of claim 27, wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit.

29. (Currently Amended) An article comprising:

a storage medium comprising machine-readable instructions encoded there on for:

having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit; ~~and~~

loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit, the instructions comprising one or more instructions to initialize the core processing circuit upon release from the reset state; and

setting an address translation unit to enable at least one outbound transaction to address at least one location in the system memory to fetch instructions from the system memory in response to requests from the core processing circuit, the address translation unit being configured to convert an internal data bus address associated with the outbound transaction to an external data bus address and configured to forward the outbound transaction from an internal data bus coupled to the core processing circuit to an external data bus coupled to the system memory.

30. (Original) The article of claim 29, wherein the storage medium further comprises machine readable instructions stored thereon for transmitting the instructions from the system memory through a host bridge of the host processing system.

31. (Original) The article of claim 29, wherein the storage medium further comprising machine readable instructions stored thereon for releasing the core processing circuit from the reset state in response to loading the instructions at the boot address.

32. (Original) The article of claim 29, wherein the storage medium further comprises machine readable instructions stored thereon for loading the instructions to a boot address in registers formed in one of a cache memory associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus.

33. (Cancelled)

34. (Previously Presented) The article of claim 29, wherein the one or more instructions comprise instructions to commence a power-on self test procedure.

35. (Previously Presented) The article of claim 34, wherein the one or more instructions further comprise instructions to launch an operating system to the core processing circuit.